



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/608,158

06/30/2000

Artur E. Balasinski

10200/82

1108

26263

7590

04/20/2004

SONNENSCHN NATH & ROSENTHAL LLP

P.O. BOX 061080

WACKER DRIVE STATION, SEARS TOWER

CHICAGO, IL 60606-1080

EXAMINER

THANGAVELU, KANDASAMY

ART UNIT

PAPER NUMBER

2123

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/608,158

Applicant(s)

BALASINSKI ET AL.

Examiner

Kandasamy Thangavelu

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This communication is in response to the Applicants' Amendment dated January 12, 2004. Claims 1 and 4 were amended. Claims 9-13 were added. Claims 1-13 of the application are pending in the application. This office action is made final.

#### ***Response to Amendments***

2. Applicants' arguments filed on January 12, 2004 have been fully considered. Applicants' arguments, filed on January 12, 2004 under 35 U.S.C. 102 (e) and 35 U.S.C. 103 (a) are not persuasive. Additional claim rejections under 35 U.S.C 103 (a) are included in this office action in response to the claim additions made. Applicants' attention is directed to response to Applicants' arguments regarding art rejections under 35 U.S.C. 102 (e) and 35 U.S.C. 103 (a) presented at Paragraph 13 below.

#### ***Drawings***

3. The draft person has objected to the drawings; see a copy of Form PTO-948 attached to paper No. 11, for an explanation.

#### ***Title***

Art Unit: 2123

4. The title says "Scheme for improving the predictability and/or reliability of photolithographic images". However, neither the specification describes the scheme for improving the ***predictability and/or reliability*** of photolithographic images nor the application claims any method or system for improving the ***predictability and/or reliability*** of photolithographic images. Therefore a change of title of the application to reflect the material described in the specification and claimed is recommended. "A scheme for improving the simulation accuracy of integrated circuit pattern by simulation of the mask" may be appropriate.

#### ***Specification***

5. The disclosure is objected to because of the following informalities:

The corrections to the specification mailed on January 12, 2004, states on Page 2, Lines 5-6, "the mask may be corrected and/or optimized and/or the simulation or image thereof may be corrected and/or optimized". However, claim 2 of January 12, 2004 states "correcting and/or optimizing the mask and/or the simulation of image thereof". The discrepancy between the specification and the claim needs to be corrected.

#### ***Claim Rejections - 35 USC § 102***

Art Unit: 2123

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by **Chang et al. (CH)** (U.S. Patent 6,470,489).

7.1 **CH** teaches Design rule checking system and method. Specifically, as per Claim 1, **CH** teaches a method comprising simulating from a drawn layout a photolithographic mask for fabrication of an integrated circuit (CL17, L26-41); then simulating an image to be produced by that mask on a wafer (Abstract, L1-7, CL4, L5-9).

Dependent claims

Per Claim 2: **CH** teaches the method of claim 1 further comprising correcting and/or optimizing the mask and/or the simulation or image thereof (CL3, L21-24; CL3, L41-43; CL4, L22-27).

Per Claim 3: **CH** teaches that the correcting and/or optimizing comprises increasing or decreasing at least one magnitude or value of (a) an optical proximity correction factor and/or (b) a serif (CL3, L41-43; CL14, L31-44).

Art Unit: 2123

7.2 As per Claim 4, **CH** teaches a method comprising simulating optical proximity effects of drawn layout for a mask for fabrication of an integrated circuit (Fig. 12; CL17, L26-41); and correcting corner rounding effects in an image produced by the mask (Fig. 7; CL14, L31-58).

7.3 As per Claim 6, **CH** teaches a method comprising incorporating corrections for corner rounding effects in an image produced by an integrated circuit mask into an optical proximity correcting procedure by adjusting an as-drawn layout of the mask as part of a computer aided design process (Fig. 7; CL14, L31-58).

Dependent claims

Per Claim 7: **CH** teaches that distortions are applied to corners and serifs in the mask (CL14, L31-58).

7.4 As per Claim 8, **CH** teaches a format for data input into or output from either or both simulating steps of claim 1, each format being compatible with the other (CL5, L21-22; CL15, L10-11; CL4, L57-60).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. (CH)** (U.S. Patent 6,470,489) in view of **Pati (PA)** ("Panel: Subwavelength lithography: How will it affect your design flow?", IEEE, 1999).

10.1 As per claim 5, **CH** teaches the method of Claim 4. **CH** does not expressly teach that the optical proximity effects comprise effects of light having a wavelength of approximately four times a feature size of the image. **PA** teaches that the optical proximity effects comprise effects of light having a wavelength of approximately four times a feature size of the image (CL1, Para 2), as these techniques offer potential for substantial speed, power and area benefits and because they are implemented through software models, the cost and time to realize these benefits are substantially smaller than equipment upgrades (CL1, Para 2). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **CH** with the method of **PA** that included the optical proximity effects comprising effects of light having a wavelength of approximately four times a feature size of the image, as these techniques offer

potential for substantial speed, power and area benefits and because they would be implemented through software models, the cost and time to realize these benefits would be substantially smaller than equipment upgrades.

11. Claims 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al. (CH)** (U.S. Patent 6,470,489) in view of **Tsukuda (TS)** (U.S. Patent 6,038,020).

11.1 As per Claim 9, **CH** teaches a method for producing a mask for fabrication of an integrated circuit (CL2, L16-19; CL2, L60-62; CL3, L1-19); comprising:

simulating a mask from a first drawn layout, to produce a simulated mask (CL17, L26-41);

wherein the simulating comprises simulating proximity effects and resolution due to pixel size (Fig. 12; CL17, L26-41).

**CH** does not expressly teach comparing the simulated mask and the first drawn layout; correcting the first drawn layout, to produce a second drawn layout; and producing a mask from the second drawn layout. **TS** teaches comparing the simulated mask and the first drawn layout; correcting the first drawn layout, to produce a second drawn layout; and producing a mask from the second drawn layout (Fig. 11; Fig 14; CL1, L37-56; CL2, L50 to CL4, L4), as that allows verifying the mask pattern generated automatically and accurately and correcting the layout, so mask pattern without any defect can be formed (CL2, L31-38; CL1, L50-572). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the



Art Unit: 2123

method of **CH** with the method of **TS** that included comparing the simulated mask and the first drawn layout; correcting the first drawn layout, to produce a second drawn layout; and producing a mask from the second drawn layout, as that would allow verifying the mask pattern generated automatically and accurately and correcting the layout, so mask pattern without any defect can be formed.

Per Claim 11: **CH** teaches the method of claim 9 further comprising simulating a photoresist pattern from the simulated mask, prior to correcting the first drawn layout (CL4, L41-43).

11.2 As per Claims 12-13, **CH** and **TS** teach the method of Claim 9. **CH** teaches a method of producing a semiconductor structure (CL2, L9-34); comprising:

producing a mask by the method of claim 9 (CL2, L16-19; CL2, L60-62; CL3, L1-19);  
and  
producing a semiconductor structure from the mask (CL2, L9-34).

**CH** teaches a method of producing an integrated circuit (CL1, L24-43); comprising:  
producing a semiconductor structure by the method of claim 12 (CL2, L9-34); and  
producing a integrated circuit from the semiconductor structure (CL1, L52-55).

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al.** (**CH**) (U.S. Patent 6,470,489) in view of **Tsukuda.** (**TS**) (U.S. Patent 6,038,020), and further in

view of **Pati (PA)** (“Panel: Subwavelength lithography: How will it affect your design flow?”, IEEE, 1999).

12.1 As per claim 10, **CH** and **TS** teach the method of Claim 9. **CH** does not expressly teach that the optical proximity effects comprise effects of light having a wavelength of approximately four times a feature size of the image. **PA** teaches that the optical proximity effects comprise effects of light having a wavelength of approximately four times a feature size of the image (CL1, Para 2), as these techniques offer potential for substantial speed, power and area benefits and because they are implemented through software models, the cost and time to realize these benefits are substantially smaller than equipment upgrades (CL1, Para 2). It would have been obvious to one of ordinary skill in the art at the time of Applicants’ invention to modify the method of **CH** with the method of **PA** that included the optical proximity effects comprising effects of light having a wavelength of approximately four times a feature size of the image, as these techniques offer potential for substantial speed, power and area benefits and because they would be implemented through software models, the cost and time to realize these benefits would be substantially smaller than equipment upgrades.

### ***Arguments***

13. As per the applicants’ arguments, the applicants’ attention is requested to the corresponding claim rejections. In addition, the following explanation is provided to further explain the examiner’s position.

13.1 As per the applicants' argument that "Chang et al. simulate photoresist patterns (i.e. the image produced by the mask), but do not produce a simulated mask from a drawn layout; ... there is no discussion about nor suggestion that, the mask itself is not the same as the ideal layout; there is no suggestion to adjust the drawn layout of the mask to take into account distortions from the mask making process", the examiner respectfully disagrees.

CH teaches producing a simulated mask from a drawn layout (CL17, L37-41). TS teaches that the mask itself is not the same as the ideal layout; there is suggestion to adjust the drawn layout of the mask to take into account distortions from the mask making process (Fig. 11; Fig 14; CL1, L37-56; CL2, L50 to CL4, L4).

13.2 As per the applicant's argument that "Pati has no suggestion to adjust the drawn layout of the mask to take into account distortions from the mask making process", the Applicants' attention is directed to Paragraph 13.1 above.

### ***Conclusion***

### ***ACTION IS FINAL***

14. Applicant's amendments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

Art Unit: 2123

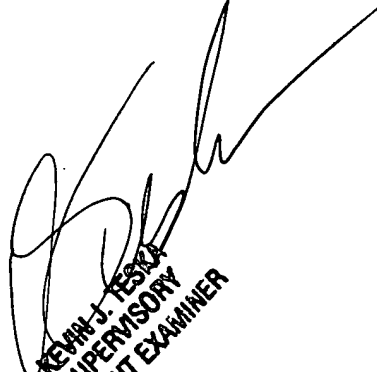
MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu  
Art Unit 2123  
April 9, 2004



KEVIN J. TESKA  
SUPERVISORY  
PATENT EXAMINER